SUBSTITUTE SPECIFICATION

TITLE OF THE INVENTION

SIMULATION APPARATUS, METHOD AND PROGRAM

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to a simulation apparatus for executing a program for a Very Long Instruction Word (VLIW) processor assisting a software developer in program development.

(2) Description of the Related Art

A simulation apparatus that simulates the simulation condition of a processor is useful in program development. A simulation apparatus for a processor that performs a pipeline control performs a pipeline simulation correctly, and thus it performs a simulation on a cycle-by-cycle basis. There is a patent literature 1 as a related art literature concerning this.

The pipeline computer simulator disclosed in this patent literature 1 performs the simulation of a step operation on an instruction-by-instruction basis while performing a pipeline simulation. By doing so, a step operation for a single instruction that is useful for a debug operation is intuitive to operate correctly.

Also, the stall detection display device disclosed in patent literature 2 detects stall that occurs in an assembler source caused by analyzing the assembler source and highlights the cause of stall occurrence on the assembler source and the part corresponding to a pipeline image which is an analysis result of the assembler source. By doing so, a programmer recognizes the cause of stall occurrence in the pipeline.

[patent literature 1]

Japanese Laid-Open Patent application No. 8-272612

[patent literature 2]

Japanese Laid-Open Patent application No. 11-65845

However, in the above-mentioned related art, a software developer cannot confirm the simulation process performed on an